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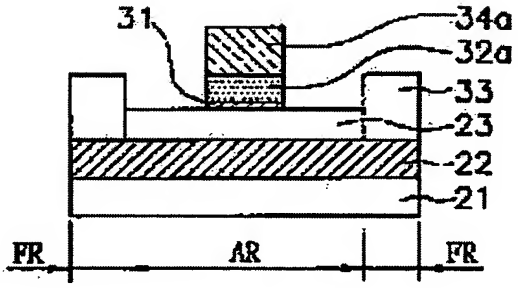
(54) SOI ELEMENT AND ITS MANUFACTURE

(57)Abstract:

PROBLEM TO BE SOLVED: To obtain an SOI element which prevents the generation of a leakage current due to a fringe effect, which prevents an increase in an OFF-leakage current and whose element characteristic and reliability are enhanced, by a constitution wherein a gate electrode is arranged only on an active region and its end parts are not covered.

SOLUTION: Since a gate-electrode pattern 32a is formed in such a way that a first conductive film which is left on an active region AR is etched, it is arranged only on the active region AR. On the other hand, a gate-electrode line 34a is arranged not only on the gate-electrode pattern 32a but also on a field region FR in such a way that it connects gate electrode patterns 32 which are arranged in a row and which are formed respectively on an adjacent active region AR. In this SOI element, a gate electrode which is composed of the gate-electrode pattern 32a and the gate-electrode line 34a is formed only on the active region AR, and a structure in which ends of the active region AR are not covered is formed. As a result, a leakage current at a time when a channel is first turned on at the ends of the active region AR is not generated.



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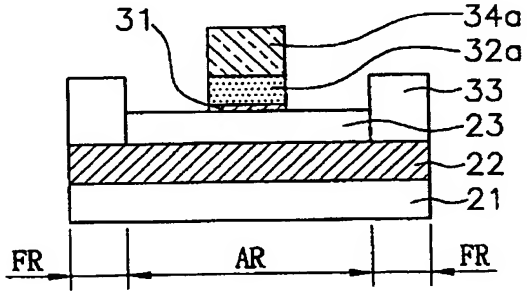
(54)【発明の名称】　ＳＯＩ素子及びその製造方法

(57)【要約】
【目的】　端部リーク電流のないＳＯＩ素子及びその製造方法を提供する。
【構成】　ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板；活性領域を限定するように、前記フィールド領域の該半導体層部分に前記埋め込み酸化膜と接するように形成された酸化膜；前記活性領域上のみに形成されたゲート酸化膜を持つゲート電極パターン；前記ゲート電極パターンの両側の前記半導体層の活性領域内に形成されたソース及びドレイン領域；及び一列に配列された活性領域の各々に形成されたゲート電極パターン間を連結するように、前記ゲート電極パターン上及びフィールド領域上に形成されたゲート電極ラインを含む。



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【特許請求の範囲】

【請求項１】　ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板；活性領域を限定するように、前記フィールド領域の該半導体層部分に前記埋め込み酸化膜と接するように形成された酸化膜；前記活性領域上のみに形成されたゲート酸化膜を持つゲート電極パターン；前記ゲート電極パターンの両側の前記半導体層の活性領域内に形成されたソース及びドレイン領域；及び、

一列に配列された活性領域の各々に形成されたゲート電極パターン間を連結するように、前記ゲート電極パターン上及びフィールド領域上に形成されたゲート電極ラインを含むことを特徴とするＳＯＩ素子。

【請求項２】　前記酸化膜は前記ソース及びドレイン領域上にも形成されることを特徴とする請求項１記載のＳＯＩ素子。

【請求項３】　前記酸化膜と前記ゲート電極パターンの上部表面の高さが同様であることを特徴とする請求項１記載のＳＯＩ素子。

【請求項４】　前記ゲート電極パターンとゲート電極ラインの材質が異なることを特徴とする請求項１記載のＳＯＩ素子。

【請求項５】　前記ゲート電極パターンはポリシリコン材質で、前記ゲート電極ラインは金属シリサイド材質であることを特徴とする請求項４記載のＳＯＩ素子。

【請求項６】　前記ゲート電極パターンと前記ゲート電極ラインの材質が同様であることを特徴とする請求項１記載のＳＯＩ素子。

【請求項７】　前記ゲート電極ラインが前記ゲート電極パターンよりも大幅であることを特徴とする請求項６記載のＳＯＩ素子。

【請求項８】　ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板を提供する段階；前記半導体層上にゲート酸化膜と第１の導電膜を順次形成する段階；活性領域が限定されるように、フィールド領域の該部分の前記第１の導電膜、ゲート酸化膜及び半導体層部分をエッチングする段階；前記結果物上に酸化膜を蒸着する段階；前記エッチングした第１の導電膜が露出するまで前記酸化膜を研磨する段階；前記エッチングした第１の導電膜と前記研磨された酸化膜上に第２の導電膜を蒸着する段階；前記第２の導電膜上にライン形態のマスクパターンを形成する段階；前記マスクパターンを用いて前記第２の導電膜、エッチングした第１の導電膜及びゲート酸化膜をエッチングすることで、前記活性領域上のみに配置されるゲート電極パターンと一列に配列された隣接する活性領域上に各々形成されたゲート電極パターンを相互連結するゲート電極ラインを形成する段階；及び、前記ゲート電極ラインの両側の前記半導体層の活性領域内に各々ソース及びドレイン領域を形成する段階を含むことを特徴とするＳＯＩ素子の製造方法。

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【請求項９】　前記ゲート電極パターンとゲート電極ラインは同じ材質で形成されることを特徴とする請求項８記載のＳＯＩ素子の製造方法。

【請求項１０】　前記ゲート電極パターンとゲート電極ラインは異なる材質で形成されることを特徴とする請求項８記載のＳＯＩ素子の製造方法。

【請求項１１】　前記ゲート電極パターンはポリシリコンで形成され、前記ゲート電極ラインは金属シリサイドで形成されることを特徴とする請求項１０記載のＳＯＩ素子の製造方法。

【請求項１２】　ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板を提供する段階；前記半導体層上にゲート酸化膜と第１の導電膜を順次形成する段階；導電ラインが形成されるように、前記第１の導電膜と前記ゲート酸化膜をパターニングする段階；前記導電ラインの両側の前記半導体層内に各々ソース及びドレイン領域を形成する段階；活性領域が限定されるように、フィールド領域上のゲート酸化膜を持つ導電ライン及び半導体層をエッチングすることで、活性領域上のみにゲート電極パターンを形成する段階；前記結果物上に酸化膜を蒸着する段階；前記ゲート電極パターンが露出するまで前記酸化膜を研磨する段階；及び、

前記ゲート電極パターン上及び酸化膜上に一列に配列された隣接する活性領域上に各々形成されたゲート電極パターンを相互連結するゲート電極ラインを形成する段階を含むことを特徴とするＳＯＩ素子の製造方法。

【請求項１３】　前記ゲート電極パターンとゲート電極ラインは同じ材質で形成されることを特徴とする請求項１２記載のＳＯＩ素子の製造方法。

【請求項１４】　前記ゲート電極ラインが前記ゲート電極パターンよりも大幅に形成されることを特徴とする請求項１３記載のＳＯＩ素子。

【請求項１５】　前記ゲート電極パターンとゲート電極ラインは異なる材質で形成されることを特徴とする請求項１２記載のＳＯＩ素子の製造方法。

【請求項１６】　前記ゲート電極パターンはポリシリコンで形成され、前記ゲート電極ラインは金属シリサイドで形成されることを特徴とする請求項１５記載のＳＯＩ素子の製造方法。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は、ＳＯＩ（Silicon-On-Insulator）素子及びその製造方法に関し、特に活性領域の端部で発生するリーク電流を抑制できるＳＯＩ素子及びその製造方法に関する。

【０００２】

【従来の技術】近年、半導体素子の高性能化に伴い、バルクシリコンからなるシリコン基板の代わりに、ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板を用いた半導体集積技術が注目されている。

これは、前記ＳＯＩ基板に形成された素子（以下、ＳＯＩ素子と称する）が、通常の単結晶シリコン基板に形成された素子と比較して、接合容量（Junction Capacitance）の減少による高速化、しきい電圧（Threshold Voltage）の減少による低電圧化、及び完全な素子分離によるラッチ－アップ（Latch-Up）の減少などの利点を持つためである。

【０００３】一方、前記ＳＯＩ素子の製造の際、活性領域を限定するための素子分離工程は通常の半導体製造工程と同様なＬＯＣＯＳまたはトレンチ方式にて行われる。合わせて、前記素子分離工程はフィールド領域の該半導体層部分を埋め込み酸化膜までエッチングするメサ分離（MESA Isolation）方式にも行われる。

【０００４】以下に前記メサ分離方式を用いて製作した従来技術によるＳＯＩ素子及びその製造方法を、図１及び図２を参照して説明する。尚、図１はその平面図であり、図２はその製造方法を説明するための図１に示すII－II´線断面図である。

【０００５】図１を参照して、活性領域ＡＲは島状を持つようにフィールド領域ＦＲの該半導体層３部分が埋め込み酸化膜２までエッチングされることにより限定される。ゲート電極１２はライン形態で具備され、横方向または縦方向に隣接する活性領域は前記ゲート電極１２によって相互に連結される。

【０００６】図２を参照して、ベース基板１、埋め込み酸化膜２及び半導体層３の積層構造からなるＳＯＩ基板１０が提供される。前記ＳＯＩ基板１０は、活性領域ＡＲ及び素子分離領域ＦＲを有し、前記活性領域ＡＲは、前記フィールド領域ＦＲの該半導体層部分が前記埋め込み酸化膜２までエッチングされることにより限定される。ゲート酸化膜１１を持つゲート電極１２が前記活性領域ＡＲの端部を覆うように前記結果物上に形成される。

【０００７】

【発明が解決しようとする課題】しかし、前記メサ分離方式を用いて製作した従来技術によるＳＯＩ素子は、前記活性領域ＡＲの端部が前記ゲート電極１２で覆われることによりリーク電流を増加させ、その結果、駆動速度の低下等の素子特性の低下を招く。

【０００８】詳しくは、メサ分離方式を用いて製作した従来のＳＯＩ素子は、図２に示すように、活性領域ＡＲの端部がゲート電極１２で覆われた形態を持つ。この場合、前記ゲート電極１２に所定電圧が印加されると、ゲートによる電場が前記活性領域ＡＲの端部に集中する現象を引き起こす。ところが、この活性領域ＡＲの端部への電場の集中は、前記活性領域ＡＲの端部に形成されるチャンネルが前記活性領域ＡＲ内側に形成されるチャンネルよりも先にターンオン（Turn-On）する現象を引き起こすため、その結果、オフリーク電流（Off-leakage Current）が増加することにより素子特性が低下する。

【０００９】図３は前記ＳＯＩ素子に対するＶＧ－ＩＤ曲線を示すグラフである。図において、実線は、端部による効果を含んだ実際ＶＧ－ＩＤ曲線を示し、点線は端部による効果を排除したＶＧ－ＩＤ曲線を示す。

【００１０】図３を参照して、活性領域の端部で発生するチャンネルがその内側部分で発生するチャンネルよりも先にターンオンすることにより、ＶＧ－ＩＤ曲線でハンプ（Hump）が発生する。また、ＶＧＳ＝０Ｖの時のオフリーク電流を比較してみれば、端部による効果が現れた場合のリーク電流が、そうでない場合のリーク電流よりも大きい。

【００１１】このように、メサ分離方式を用いてＳＯＩ素子を製造する場合、端部効果によるリーク電流の増加を防止することが、素子特性低下を解決する必須の課題である。

【００１２】本発明は前記課題を解決するために創案されたものであり、その目的は、端部リーク電流のないＳＯＩ素子を提供することである。また、本発明の他の目的は、端部リーク電流のないＳＯＩ素子の製造方法を提供することである。

【００１３】

【課題を解決するための手段】前記目的を達成するために本発明によるＳＯＩ素子は、ベース基板、埋め込み酸化膜、及び半導体層の積層構造からなるＳＯＩ基板；活性領域を限定するように、前記フィールド領域の該半導体層部分に前記埋め込み酸化膜と接するように形成された酸化膜；前記活性領域上のみに形成されたゲート酸化膜を持つゲート電極パターン；前記ゲート電極パターンの両側の前記半導体層の活性領域内に形成されたソース及びドレイン領域；及び一列に配列された活性領域の各々に形成されたゲート電極パターン間を連結するように、前記ゲート電極パターン上及びフィールド領域上に形成されたゲート電極ラインを含む。

【００１４】また、本発明によるＳＯＩ素子の製造方法は、ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板を提供する段階；前記半導体層上にゲート酸化膜と第１の導電膜を順次形成する段階；活性領域が限定されるように、フィールド領域の該部分の前記第１の導電膜、ゲート酸化膜及び半導体層部分をエッチングする段階；前記結果物上に酸化膜を蒸着する段階；前記エッチングした第１の導電膜が露出するまで前記酸化膜を研磨する段階；前記エッチングした第１の導電膜と前記研磨された酸化膜上に第２の導電膜を蒸着する段階；前記第２の導電膜上にライン形態のマスクパターンを形成する段階；前記マスクパターンを用いて前記第２の導電膜、エッチングした第１の導電膜及びゲート酸化膜をエッチングすることで、前記活性領域上のみに配置されるゲート電極パターンと一列に配列された隣接する活性領域上に各々形成されたゲート電極パターンを

相互連結するゲート電極ラインを形成する段階；及び前記ゲート電極ラインの両側の前記半導体層の活性領域内に各々ソース及びドレイン領域を形成する段階を含む。

【００１５】さらに、本発明によるＳＯＩ素子の製造方法は、ベース基板、埋め込み酸化膜及び半導体層の積層構造からなるＳＯＩ基板を提供する段階；前記半導体層上にゲート酸化膜と第１の導電膜を順次形成する段階；導電ラインが形成されるように、前記第１の導電膜と前記ゲート酸化膜をパターニングする段階；前記導電ラインの両側の前記半導体層内に各々ソース及びドレイン領域を形成する段階；活性領域が限定されるように、フィールド領域上のゲート酸化膜を持つ導電ライン及び半導体層をエッチングすることで、活性領域上のみにゲート電極パターンを形成する段階；前記結果物上に酸化膜を蒸着する段階；前記ゲート電極パターンが露出するまで前記酸化膜を研磨する段階；及び前記ゲート電極パターン上及び酸化膜上に一列に配列された隣接する活性領域上に各々形成されたゲート電極パターンを相互連結するゲート電極ラインを形成する段階を含む。

【００１６】本発明及びその実施の形態は、以下の説明及び図面を参照することにより、より良く理解可能となる。

【００１７】

【発明の実施の形態】以下、添付図面に基づいて、本発明の好適実施例を詳細に説明する。図４乃至図９は本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【００１８】図４を参照して、全体を支持するベース基板２１、前記ベース基板２１上に配置されて完全な素子分離を提供する埋め込み酸化膜２２、及び前記埋め込み酸化膜２２上に配置されて活性領域を提供する半導体層２３の積層構造からなるＳＯＩ基板３０が提供される。前記ＳＯＩ基板３０は、活性領域ＡＲ及びフィールド領域ＦＲを持つ。前記半導体層２３は１００～５，０００Ａの厚さを持つことが望ましい。ゲート酸化膜３１が前記半導体層２３上に形成され、第１の導電膜３２が前記ゲート酸化膜３１上に蒸着される。前記第１の導電膜３２は、望ましくはポリシリコン膜である。

【００１９】図５を参照して、素子が形成される活性領域ＡＲがフィールド領域ＦＲ上に形成された第１の導電膜部分、ゲート酸化膜部分及び半導体層部分を、前記埋め込み酸化膜２２が露出するまでエッチングするメサ分離方式により限定される。図１０は、図５に対応する平面図である。図に示すように、前記エッチングした第１の導電膜３２は前記活性領域ＡＲ上のみに残留する。

【００２０】図６を参照して、酸化膜３３が前記エッチングした第１の導電膜３２を完全に覆う程度の充分な厚さで前記結果物上に蒸着される。その後、前記酸化膜３３は前記エッチングした第１の導電膜３２が露出するまでＣＭＰ（Chemical Mechanical Polishing）工程により研磨される。この結果、前記酸化膜３３はフィールド領域ＦＲ上のみに残留する。

【００２１】図７を参照して、第２の導電膜３４が前記研磨された酸化膜３３及び前記エッチングした第１の導電膜３２上に蒸着される。ここで、前記第２の導電膜３４は、前記第１の導電膜３２と同じ物質であるか、或いは異なる物質である。例えば、前記第１の導電膜３２がポリシリコン膜であれば、前記第２の導電膜３４は金属シリサイド膜であるのが望ましい。フォトレジストからなるマスクパターン３５が前記第２の導電膜３４上にライン形態で形成される。

【００２２】図８を参照して、ゲート電極ライン３４ａ及びゲート電極パターン３２ａがエッチングマスクとして前記マスクパターン（不図示）を用いて第２の導電膜、第１の導電膜及びゲート酸化膜をエッチングすることにより形成される。しかる後に、前記マスクパターンは除去される。

【００２３】ここで、前記ゲート電極パターン３２ａは活性領域ＡＲ上に残留した第１の導電膜がエッチングされることにより形成されるため、前記活性領域ＡＲ上のみに配置される。反面、前記ゲート電極ライン３４ａは一列に配列された隣接する活性領域ＡＲ上に各々形成されたゲート電極パターン間を相互に連結するように、前記ゲート電極パターン３２ａ上は勿論、フィールド領域ＦＲ上にも配置される〔図１１（ａ），１１（ｂ）〕。

【００２４】図９を参照して、ソース及びドレイン領域３６、３７が、マスクとして前記ゲート電極ライン３４ａを用いるイオン注入工程によって前記ゲート電極ライン３４ａの両側の半導体層部分内に形成される。この結果、トランジスタのようなＳＯＩ素子が完成する。

【００２５】前記工程により製作した本発明によるＳＯＩ素子において、ゲート電極パターンとゲート電極ラインからなるゲート電極は、活性領域上のみに形成されるだけで、活性領域の端部を覆わない構造に形成されるため、前記活性領域の端部でチャンネルが先にターンオンされることによるリーク電流は発生しない。よって、本発明によるＳＯＩ素子は端部効果によるオフリーク電流の増加を防止できるために、その特性及び信頼性を向上させることができる。

【００２６】図１２乃至図１６は本発明の他の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。ここで、先の実施例と同じ部分は同一の符号にて示す。

【００２７】図１２を参照して、ベース基板２１、埋め込み酸化膜２２及び半導体層２３の積層構造からなるＳＯＩ基板３０が提供され、ゲート酸化膜３１、及び第１の導電膜４２が前記半導体層２３上に順次形成される。前記第１の導電膜４２及びゲート酸化膜３１はライン形態を持つようにパターニングされる（図１７参照）。

【００２８】ソース及びドレイン領域３６、３７がマス

クとして前記パターニングされた第１の導電膜４２を用いるイオン注入工程によって前記第１の導電膜４２の両側の半導体層部分内に形成される。

【００２９】図１３を参照して、フォトレジストからなるマスクパターン５０が前記結果物上に活性領域ＡＲを覆うように形成される。

【００３０】図１４を参照して、活性領域ＡＲは前記マスクパターン（不図示）を用いて露出した半導体層部分を埋め込み酸化膜２２が露出するまでエッチングすることにより限定される。このとき、前記エッチングの間に、フィールド領域ＦＲ上に形成された第１の導電膜及びゲート酸化膜部分が共にエッチングされ、この結果、ゲート酸化膜を持つゲート電極パターン４２ａが前記活性領域ＡＲ上のみに配置されるように形成される。しかる後に、前記マスクパターンは除去される。

【００３１】図１８は前記工程の結果を示す前記図１４に対応する平面図である。図に示すように、前記ゲート電極パターン４２ａは活性領域ＡＲ上のみに配置される。

【００３２】図１５を参照して、酸化膜３３が前記結果物上に蒸着され、その後、前記ゲート電極パターン４２ａの上面が露出するまでＣＭＰ工程により研磨される。

【００３３】図１６を参照して、第２の導電膜が前記結果物上に蒸着され、その後、ゲート電極ライン４４ａは前記第２の導電膜がパターニングされることにより形成される。前記ゲート電極ライン４４ａは先の実施例と同様に、一列に配列された隣接する活性領域ＡＲ上に各々形成されたゲート電極パターンを相互連結するように形成される。

【００３４】前記ゲート電極ライン４４ａは、前記ゲート電極パターン４２ａと異なる材質で形成することができる。例えば、前記ゲート電極パターン４２ａがポリシリコン膜で形成された場合、前記ゲート電極ライン４４ａは金属シリサイド膜で形成するのが望ましい。

【００３５】また、前記ゲート電極ライン４４ａは、前記ゲート電極パターン４２ａと同じ材質で形成することができる。この場合、前記ゲート電極ライン４４ａを形成するためのエッチング時に、誤整列により図１９に示す様なゲート酸化膜３１が露出するため、素子の信頼性が低下する。よって、前記ゲートライン４４ａは前記ゲート電極パターン４２ａと同じ材質で形成される場合、誤整列によるゲート酸化膜３１の露出が防止される様に、前記ゲート電極パターン４２ａよりも大幅に形成されるのが望ましい。

【００３６】尚、本発明は前記実施例に限定されず、本発明の趣旨から逸脱しない範囲内で多様に変更実施することが可能である。

【００３７】

【発明の効果】以上説明のように本発明は、ゲート電極が活性領域上のみに配置されて、その端部を覆わないように構成したことから、端部効果によるリーク電流の発生を防止できる。これにより、オフリーク電流の増加を防止でき、素子特性及び信頼性を向上させることができる。

【図面の簡単な説明】

【図１】メサ分離方式を用いて製作した従来技術によるＳＯＩ素子を示す平面図である。

【図２】前記ＳＯＩ素子の製造方法を説明するための図１に示すII－II´線に沿う断面図である。

【図３】ゲート電圧に対するドレイン電流の変化を示すＶＧ－ＩＤ曲線である。

【図４】本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図５】本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図６】本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図７】本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図８】本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図９】本発明の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図１０】図５に対応する平面図である。

【図１１】（ａ）は、図８に対応する平面図であり、（ｂ）は、（ａ）のＹ－Ｙ´線に沿う断面図である。

【図１２】本発明の他の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図１３】本発明の他の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図１４】本発明の他の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図１５】本発明の他の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図１６】本発明の他の実施例によるＳＯＩ素子の製造方法を説明するための断面図である。

【図１７】図１２に対応する平面図である。

【図１８】図１４に対応する平面図である。

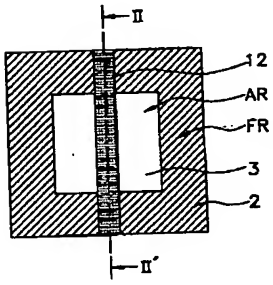
【図１９】本発明の他の実施例により形成されたゲート電極ラインとゲート電パターンとの間の誤整列が発生した状態を示す断面図である。

【符号の説明】

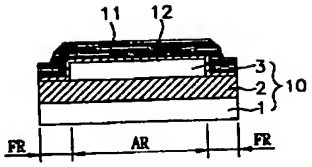
２１　ベース基板
２２　埋め込み酸化膜
２３　半導体層
３０　ＳＯＩ基板
３１　ゲート酸化膜
３２、４２　第１の導電膜
３２ａ、４２ａ　ゲート電極パターン
３３　酸化膜

３４　第２の導電膜
３４ａ、４４ａ　ゲート電極ライン
３５、５０　マスクパターン
＊３６　ソース領域
３７　ドレイン領域

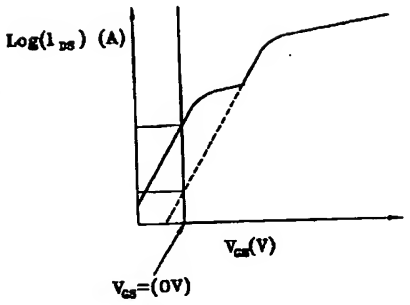
【図１】



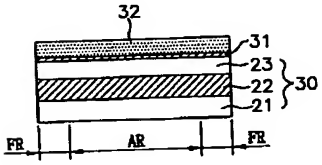
【図２】



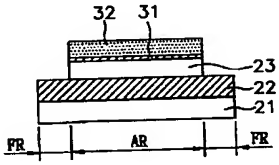
【図３】



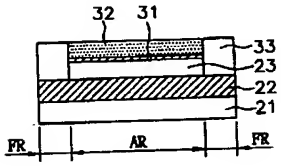
【図４】



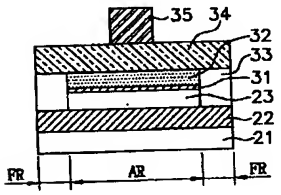
【図５】



【図６】



【図７】



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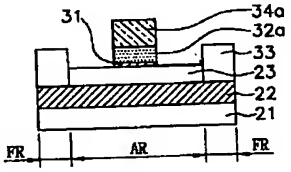

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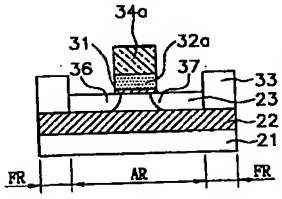
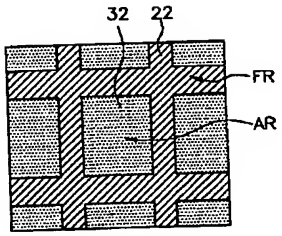
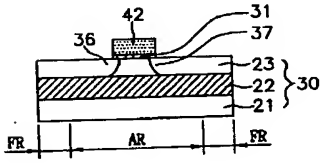


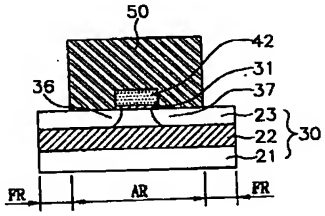
【図１０】



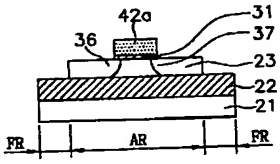
【図１２】



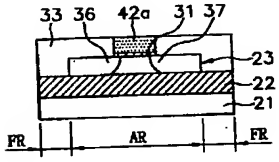
【図１３】



【図１４】

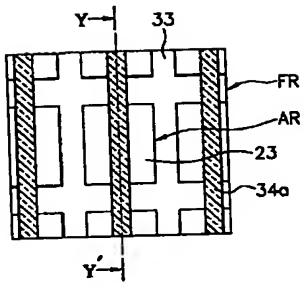


【図１５】

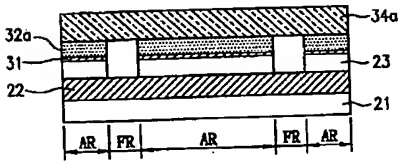


【図１１】

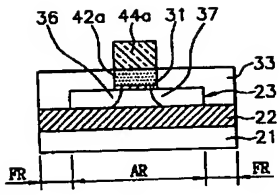
(a)



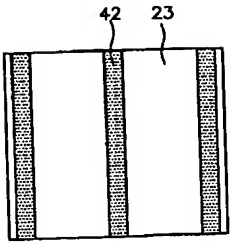
(b)



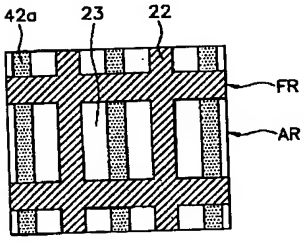
【図１６】



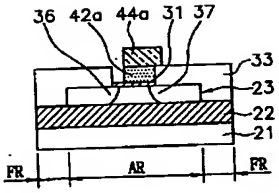
【図１７】



【図１８】



【図１９】



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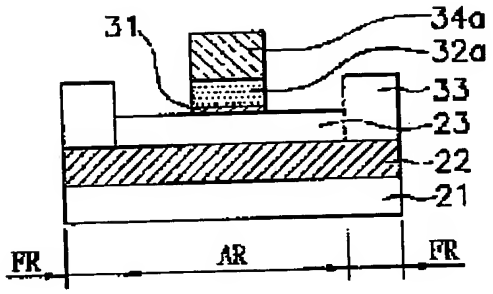
(72)Inventor : RI GENCHO
RI UKAN

(30)Priority
Priority number : 99 9924612 Priority date : 28.06.1999 Priority country : KR

(54) SOI ELEMENT AND ITS MANUFACTURE

(57)Abstract:
PROBLEM TO BE SOLVED: To obtain an SOI element which prevents the generation of a leakage current due to a fringe effect, which prevents an increase in an OFF-leakage current and whose element characteristic and reliability are enhanced, by a constitution wherein a gate electrode is arranged only on an active region and its end parts are not covered.
SOLUTION: Since a gate-electrode pattern 32a is formed in such a way that a first conductive film which is left on an active region AR is etched, it is arranged only on the active region AR. On the other hand, a gate-electrode line 34a is arranged not only on the gate-electrode pattern 32a but also on a field region FR in such a way that it connects gate electrode patterns 32 which are arranged in a row and which are formed respectively on an adjacent active region AR. In this SOI element, a gate electrode which is composed of the gate-electrode pattern 32a and the gate-electrode line 34a is formed only on the active region AR, and a structure in which ends of the active region AR are not covered is formed. As a result, a leakage current at a time when a channel is first turned on at the ends of the active region AR is not generated.



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CLAIMS

[Claim(s)]
[Claim 1] The SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an active region may be limited So that a part for this semiconductor layer of the aforementioned field field may be touched with the aforementioned embedding oxide film The source and the drain field which were formed in the active region of the aforementioned semiconductor layer of the both sides of the gate electrode pattern; aforementioned gate electrode pattern with the gate oxide film formed only on the formed oxide-film; aforementioned active region; It reaches. The silicon-on-insulator desubstrate characterized by including the gate electrode line formed on the aforementioned gate electrode pattern and the field field so that between the gate electrode patterns formed in each of the active region arranged by the single tier may be connected.
[Claim 2] The aforementioned oxide film is a silicon-on-insulator desubstrate according to claim 1 characterized by being formed also on the aforementioned source and a drain field.
[Claim 3] The silicon-on-insulator desubstrate according to claim 1 characterized by the height on the front face of up of the aforementioned oxide film and the aforementioned gate electrode pattern being the same.
[Claim 4] The silicon-on-insulator desubstrate according to claim 1 characterized by the quality of the materials of the aforementioned gate electrode pattern and a gate electrode line differing.
[Claim 5] The aforementioned gate electrode pattern is a silicon-on-insulator desubstrate according to claim 4 characterized by the aforementioned gate electrode line being the metal silicide quality of the material with the polysilicon contest quality of the material.
[Claim 6] The silicon-on-insulator desubstrate according to claim 1 characterized by the quality of the material of the aforementioned gate electrode pattern and the aforementioned gate electrode line being the same.
[Claim 7] The silicon-on-insulator desubstrate according to claim 6 characterized by the aforementioned gate electrode line being larger than the aforementioned gate electrode pattern.
[Claim 8] The stage which forms a gate oxide film and the 1st electric conduction film one by one on the stage; aforementioned semiconductor layer which offers the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an active region may be limited The electric conduction film of the above 1st of this portion of a field field, The stage which carries out the vacuum evaporationo of the oxide film to the stage; aforementioned result lifter which **********s a part for a gate oxide film and a semiconductor layer; until the 1st electric conduction film which carried out [aforementioned] etching is exposed The aforementioned mask pattern is used. The stage which forms the mask pattern of a line form on the electric conduction film of the stage; above 2nd which carries out the vacuum evaporationo of the 2nd electric conduction film on the oxide film by which polish was carried out [aforementioned] with the 1st electric conduction film which ground the aforementioned oxide film and carried out the stage; aforementioned etching; The electric conduction film of the above 2nd, By **********ing, the 1st electric conduction film and gate oxide film which **********ed The stage which forms the gate electrode line which links the gate electrode pattern arranged only on the aforementioned active region, and the gate electrode pattern respectively formed on the adjoining active region arranged by the single tier; It reaches. The manufacture method of the silicon-on-insulator desubstrate characterized by including the stage which forms the source and a drain field respectively in the active region of the aforementioned semiconductor layer of the both sides of the aforementioned gate electrode line.
[Claim 9] The aforementioned gate electrode pattern and a gate electrode line are the manufacture method of the silicon-on-insulator desubstrate according to claim 8 characterized by being formed with the same quality of the material.
[Claim 10] The aforementioned gate electrode pattern and a gate electrode line are the manufacture method of the silicon-on-insulator desubstrate according to claim 8 characterized by being formed with the different quality of the material.
[Claim 11] It is the manufacture method of the silicon-on-insulator desubstrate according to claim 10 characterized by forming the aforementioned gate electrode pattern with contest polysilicon, and forming the aforementioned gate electrode line by metal silicide.
[Claim 12] The stage which forms a gate oxide film and the 1st electric conduction film one by one on the stage; aforementioned semiconductor layer which offers the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an electric conduction line may be formed The stage which forms the source and a drain field respectively in the aforementioned semiconductor layer of the both sides of the stage; aforementioned electric conduction line which carries out patterning of the electric conduction film and the aforementioned gate oxide film of the above 1st; so that an active region may be limited By **********ing, an electric conduction line and a semiconductor layer with the gate oxide film on a field field The stage which grinds the aforementioned oxide film until the stage; aforementioned gate electrode pattern which carries out the vacuum evaporationo of the oxide film to the stage; aforementioned result lifter which forms a gate electrode pattern only on an active region is exposed; It reaches. The manufacture method of the silicon-on-insulator desubstrate characterized by including the stage which forms the gate electrode line which links the gate electrode pattern respectively formed on the adjoining active region arranged by the single tier on the aforementioned gate electrode pattern and the oxide film.
[Claim 13] The aforementioned gate electrode pattern and a gate electrode line are the manufacture method of the silicon-on-insulator desubstrate according to claim 12 characterized by being formed with the same quality of the material.
[Claim 14] The silicon-on-insulator desubstrate according to claim 13 characterized by forming the aforementioned gate electrode line more sharply than the aforementioned gate electrode pattern.
[Claim 15] The aforementioned gate electrode pattern and a gate electrode line are the manufacture method of the silicon-on-insulator desubstrate according to claim 12 characterized by being formed with the different quality of the material.
[Claim 16] It is the manufacture method of the silicon-on-insulator desubstrate according to claim 15 characterized by forming the aforementioned gate electrode pattern with contest polysilicon, and forming the aforementioned gate electrode line by metal silicide.

[Translation done.]

DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[The technical field to which invention belongs] Especially this invention relates to the silicon-on-insulator desubstrate which can suppress the leakage current generated at the edge of an active region, and its manufacture method about a SOI (Silicon-On-Insulator) element and its manufacture method.
[0002]
[Description of the Prior Art] In recent years, the semiconductor accumulation technology using the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer attracts attention with highly-efficient-izing of a semiconductor device instead of the silicon substrate which consists of bulk silicon. This is because the element (a silicon-on-insulator desubstrate is called hereafter) formed in the aforementioned SOI substrate has advantages, such as reduction of improvement in the speed by reduction in a junction capacitance (Junction Capacitance), low-battery-izing by reduction in threshold voltage (Threshold Voltage), and the latch-rise (Latch-Up) by perfect isolation, as compared with the element formed in the usual single-crystal-silicon substrate.
[0003] On the other hand, the isolation process for limiting an active region is performed by the same usual LOCOS or same usual trench format as a semiconductor manufacturing process in the case of manufacture of the aforementioned silicon-on-insulator desubstrate. It doubles and the aforementioned isolation process is performed also to the mesa separation (MESA Isolation) method which embeds a part for this semiconductor layer of a field field, and **********s to an oxide film.
[0004] The silicon-on-insulator desubstrate by the conventional technology which used and manufactured the aforementioned mesa separation method below, and its manufacture method are explained with reference to drawing 1 and drawing 2 . In addition, drawing 1 is the plan and drawing 2 is an II-II'line cross section shown in drawing 1 for explaining the manufacture method.
[0005] With reference to drawing 1 , an active region AR is limited by this semiconductor layer 3 portion of the field field FR embedding, and **********ing to an oxide film 2 so that it may have the shape of an island. The gate electrode 12 is provided with a line gestalt, and the active region which adjoins a longitudinal direction or lengthwise is mutually connected by the aforementioned gate electrode 12.
[0006] With reference to drawing 2 , the SOI substrate 10 which consists of a laminated structure of the base substrate 1, the embedding oxide film 2, and the semiconductor layer 3 is offered. The aforementioned SOI substrate 10 has an active region AR and the isolation field FR, and the aforementioned active region AR is limited by a part for this semiconductor layer of the aforementioned field field FR **********ing to the aforementioned embedding oxide film 2. It is formed in the aforementioned result lifter so that the gate electrode 12 with the gate oxide film 11 may cover the edge of the aforementioned active region AR.
[0007]
[Problem(s) to be Solved by the Invention] However, by covering the edge of the aforementioned active region AR by the aforementioned gate electrode 12, the silicon-on-insulator desubstrate by the conventional technology manufactured using the aforementioned mesa separation method makes a leakage current increase, consequently causes the fall of element properties, such as a fall of drive speed.
[0008] In detail, the conventional silicon-on-insulator desubstrate manufactured using the mesa separation method has the gestalt by which the edge of an active region AR was covered by the gate electrode 12, as shown in drawing 2 . In this case, if predetermined voltage is impressed to the aforementioned gate electrode 12, the phenomenon which the electric field by the gate concentrate on the edge of the aforementioned active region AR will be caused. However, in order that concentration of the electric field to the edge of this active region AR may cause the phenomenon in which the channel formed in the edge of the aforementioned active region AR carries out a turn-on (Turn-On) ahead of the channel formed in the aforementioned active-region AR inside consequently, when an OFF leakage current (Off-leakage Current) increases, an element property falls.
[0009] Drawing 3 is a graph which shows the VG-ID curve to the aforementioned silicon-on-insulator desubstrate. In drawing, a solid line shows an actual VG-ID curve including the effect by the edge, and a dotted line shows the VG-ID curve which eliminated the effect by the edge.
[0010] When the channel generated at the edge of an active region carries out a turn-on ahead of the channel generated in the inside portion with reference to drawing 3 , a hump (Hump) occurs with an VG-ID curve. Moreover, if the OFF leakage current at the time of VGS=0V is compared, a leakage current when the effect by the edge shows up is larger than a leakage current when that is not right.
[0011] Thus, when manufacturing a silicon-on-insulator desubstrate using a mesa separation method, preventing the increase in the leakage current by the edge effect is the indispensable technical problem which solves an element property fall.
[0012] Originated in order that this invention may solve the aforementioned technical problem, the purpose is offering a silicon-on-insulator desubstrate without an edge leakage current. Moreover, other purposes of this invention are offering the manufacture method of a silicon-on-insulator desubstrate without an edge leakage current.
[0013]
[Means for Solving the Problem] In order to attain the aforementioned purpose, the silicon-on-insulator desubstrate by this invention A base substrate, an embedding oxide film, and the SOI substrate that consists of a laminated structure of a semiconductor layer; so that an active region may be limited So that a part for this semiconductor layer of the aforementioned field field may be touched with the aforementioned embedding oxide film Formed oxide-film; A gate electrode pattern with the gate oxide film formed only on the aforementioned active region; so that between the gate electrode patterns formed in each of the active region arranged by source and drain field; and the single tier which were formed in the active region of the aforementioned semiconductor layer of the both sides of the aforementioned gate electrode pattern may be connected The gate electrode line formed on the aforementioned gate electrode pattern and the field field is included.

[0014] Moreover, the manufacture method of the silicon-on-insulator desubstrate by this invention The stage which forms a gate oxide film and the 1st electric conduction film one by one on the stage; aforementioned semiconductor layer which offers the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an active region may be limited The electric conduction film of the above 1st of this portion of a field field, The stage which carries out the vacuum evaporationo of the oxide film to the stage; aforementioned result lifter which **********s a part for a gate oxide film and a semiconductor layer; until the 1st electric conduction film which carried out [aforementioned] etching is exposed The aforementioned mask pattern is used. The stage which forms the mask pattern of a line gestalt on the electric conduction film of the stage; above 2nd which carries out the vacuum evaporationo of the 2nd electric conduction film on the oxide film by which polish was carried out [aforementioned] with the 1st electric conduction film which ground the aforementioned oxide film and carried out the stage; aforementioned etching; The electric conduction film of the above 2nd, By **********ing, the 1st electric conduction film and gate oxide film which **********ed In the active region of the aforementioned semiconductor layer of the both sides of stage; which forms the gate electrode line which links the gate electrode pattern arranged only on the aforementioned active region, and the gate electrode pattern respectively formed on the adjoining active region arranged by the single tier, and the aforementioned gate electrode line, respectively The source And the stage which forms a drain field is included.

[0015] Furthermore, the manufacture method of the silicon-on-insulator desubstrate by this invention The stage which forms a gate oxide film and the 1st electric conduction film one by one on the stage; aforementioned semiconductor layer which offers the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an electric conduction line may be formed The stage which forms the source and a drain field respectively in the aforementioned semiconductor layer of the both sides of the stage; aforementioned electric conduction line which carries out patterning of the electric conduction film and the aforementioned gate oxide film of the above 1st; so that an active region may be limited By **********ing, an electric conduction line and a semiconductor layer with the gate oxide film on a field field The stage which carries out the vacuum evaporationo of the oxide film to the stage; aforementioned result lifter which forms a gate electrode pattern only on an active region; until the aforementioned gate electrode pattern is exposed The stage which forms the gate electrode line which links the gate electrode pattern respectively formed on the adjoining active region arranged by the single tier on stage; which grinds the aforementioned oxide film, the aforementioned gate electrode pattern, and the oxide film is included.

[0016] By referring to the following explanation and a drawing, it is better and an understanding of this invention and the gestalt of the operation is attained.

[0017]

[Embodiments of the Invention] Hereafter, based on an accompanying drawing, the suitable example of this invention is explained in detail. Drawing 4 or drawing 9 is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.

[0018] The SOI substrate 30 which consists of a laminated structure of the semiconductor layer 23 which is arranged on the embedding oxide film 22 which is arranged with reference to drawing 4 on the base substrate 21 which supports the whole, and the aforementioned base substrate 21, and offers perfect isolation, and the aforementioned embedding oxide film 22, and offers an active region is offered. The aforementioned SOI substrate 30 has an active region AR and the field field FR. As for the aforementioned semiconductor layer 23, it is desirable to have the thickness of 100-5,000A. The gate oxide film 31 is formed on the aforementioned semiconductor layer 23, and the vacuum evaporationo of the 1st electric conduction film 32 is carried out on the aforementioned gate oxide film 31. The electric conduction film 32 of the above 1st is a polysilicon contest film desirably.

[0019] It is limited by the mesa separation method which **********s until the aforementioned embedding oxide film 22 exposes a part for the 1st electric conduction film portion by which the active region AR in which an element is formed was formed on the field field FR, a gate oxide-film portion, and a semiconductor layer with reference to drawing 5 . Drawing 10 is a plan corresponding to drawing 5 . As shown in drawing, the 1st electric conduction film 32 which carried out [aforementioned] etching remains only on the aforementioned active region AR.

[0020] With reference to drawing 6 , the vacuum evaporationo of the 1st electric conduction film 32 in which the oxide film 33 carried out [aforementioned] etching is completely carried out to the aforementioned result lifter by sufficient thickness about a wrap. Then, the aforementioned oxide film 33 is ground by the CMP (Chemical Mechanical Polishing) process until the 1st electric conduction film 32 which carried out [aforementioned] etching is exposed. Consequently, the aforementioned oxide film 33 remains only on the field field FR.

[0021] With reference to drawing 7 , vacuum evaporationo is carried out on the oxide film 33 and the 1st electric conduction film 32 which carried out [aforementioned] etching with which polish of the 2nd electric conduction film 34 was carried out [aforementioned]. Here, the electric conduction film 34 of the above 2nd is matter which is the same matter as the electric conduction film 32 of the above 1st, or is different. For example, if the electric conduction film 32 of the above 1st is a polysilicon contest film, as for the electric conduction film 34 of the above 2nd, it is desirable that it is a metal silicide film. The mask pattern 35 which consists of a photoresist is formed with a line gestalt on the electric conduction film 34 of the above 2nd.

[0022] With reference to drawing 8 , when gate electrode line 34a and gate electrode pattern 32a ********** the 2nd electric conduction film, the 1st electric conduction film, and a gate oxide film, using the aforementioned mask pattern (un-illustrating) as an etching mask, it is formed. After an appropriate time, the aforementioned mask pattern is removed.

[0023] Here, since the 1st electric conduction film which remained on the active region AR is formed by **********ing, the aforementioned gate electrode pattern 32a is arranged only on the aforementioned active region AR. On the other hand, the aforementioned gate electrode line 34a is arranged also on the field field FR as well as an aforementioned gate electrode pattern 32a top so that between the gate electrode patterns respectively formed on the adjoining active region AR arranged by the single tier may be connected mutually [drawing 11 (a) and 11 (b)].

[0024] With reference to drawing 9 , the source and the drain fields 36 and 37 are formed in the semiconductor layer part of the both sides of the aforementioned gate electrode line 34a of the ion-implantation process using the aforementioned gate electrode line 34a as a mask. Consequently, a silicon-on-insulator desubstrate like a transistor is completed.

[0025] In the silicon-on-insulator desubstrate by this invention manufactured according to the aforementioned process, since the gate electrode which consists of a gate electrode pattern and a gate electrode line is only formed only on an active region and is formed in the structure which does not cover the edge of an active region, the leakage current by the turn-on of the channel being previously carried out at the edge of the aforementioned active region is not generated. Therefore, since the silicon-on-insulator desubstrate by this invention can prevent the increase in the OFF leakage current by the edge effect, it can raise the property and reliability.

[0026] Drawing 12 or drawing 16 is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention. Here, the same sign shows the same portion as a previous example.

[0027] With reference to drawing 12 , the SOI substrate 30 which consists of a laminated structure of the base substrate 21, the

embedding oxide film 22, and the semiconductor layer 23 is offered, and the gate oxide film 31 and the 1st electric conduction film 42 are formed one by one on the aforementioned semiconductor layer 23. Patterning of the electric conduction film 42 and the gate oxide film 31 of the above 1st is carried out so that it may have a line form (refer to drawing 17).

[0028] The source and the drain fields 36 and 37 are formed in the semiconductor layer part of the both sides of the electric conduction film 42 of the above 1st of the ion-implantation process using the 1st electric conduction film 42 by which patterning was carried out [aforementioned] as a mask.

[0029] It is formed so that the mask pattern 50 which consists of a photoresist may cover an active region AR to the aforementioned result lifter with reference to drawing 13 .

[0030] With reference to drawing 14 , an active region AR is limited by **********ing until it embeds a part for the semiconductor layer exposed using the aforementioned mask pattern (un-illustrating) and an oxide film 22 is exposed. At this time, between the aforementioned etching, it is formed so that gate electrode pattern 42a in which it **********s, consequently the 1st electric conduction film and gate oxide-film portion which were formed on the field field FR have [both] a gate oxide film may be arranged only on the aforementioned active region AR. After an appropriate time, the aforementioned mask pattern is removed.

[0031] Drawing 18 is a plan corresponding to aforementioned drawing 14 which shows the result of the aforementioned process. As shown in drawing, the aforementioned gate electrode pattern 42a is arranged only on an active region AR.

[0032] With reference to drawing 15 , the vacuum evaporationo of the oxide film 33 is carried out to the aforementioned result lifter, and it is ground by the CMP process until the upper surface of the aforementioned gate electrode pattern 42a is exposed after that.

[0033] With reference to drawing 16 , the vacuum evaporationo of the 2nd electric conduction film is carried out to the aforementioned result lifter, and gate electrode line 44a is formed by carrying out patterning of the electric conduction film of the above 2nd after that. The aforementioned gate electrode line 44a is formed so that the gate electrode pattern respectively formed on the adjoining active region AR arranged by the single tier like the previous example may be linked.

[0034] The aforementioned gate electrode line 44a can be formed with the different quality of the material from the aforementioned gate electrode pattern 42a. For example, when the aforementioned gate electrode pattern 42a is formed by the polysilicon contest film, as for the aforementioned gate electrode line 44a, forming by the metal silicide film is desirable.

[0035] Moreover, the aforementioned gate electrode line 44a can be formed with the same quality of the material as the aforementioned gate electrode pattern 42a. In this case, since the gate oxide film 31 as shown in drawing 19 by incorrect alignment is exposed at the time of etching for forming the aforementioned gate electrode line 44a, the reliability of an element falls. Therefore, when formed with the same quality of the material as the aforementioned gate electrode pattern 42a, it is desirable [the aforementioned gate line 44a] to be formed more sharply than the aforementioned gate electrode pattern 42a so that exposure of the gate oxide film 31 by incorrect alignment may be prevented.

[0036] In addition, it is possible to Oshi to carry out change implementation within limits which this invention is not limited to the aforementioned example and do not deviate from the meaning of this invention.

[0037]

[Effect of the Invention] Above, like explanation, a gate electrode is arranged only on an active region, and since this invention was constituted so that the edge might not be covered, it can prevent generating of the leakage current by the edge effect. Thereby, the increase in an OFF leakage current can be prevented and an element property and reliability can be raised.

[Translation done.]

* NOTICES *

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2. **** shows the word which can not be translated.
3.In the drawings, any words are not translated.

TECHNICAL FIELD

[The technical field to which invention belongs] Especially this invention relates to the silicon-on-insulator desubstrate which can suppress the leakage current generated at the edge of an active region, and its manufacture method about a SOI (Silicon-On-Insulator) element and its manufacture method.

[Translation done.]

PRIOR ART

[Description of the Prior Art] In recent years, the semiconductor accumulation technology using the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer attracts attention with highly-efficient-izing of a semiconductor device instead of the silicon substrate which consists of bulk silicon. This is because the element (a silicon-on-insulator desubstrate is called hereafter) formed in the aforementioned SOI substrate has advantages, such as reduction of improvement in the speed by reduction in a junction capacitance (Junction Capacitance), low-battery-izing by reduction in threshold voltage (Threshold Voltage), and the latch-rise (Latch-Up) by perfect isolation, as compared with the element formed in the usual single-crystal-silicon substrate.

[0003] On the other hand, the isolation process for limiting an active region is performed by the same usual LOCOS or same usual trench format as a semiconductor manufacturing process in the case of manufacture of the aforementioned silicon-on-insulator desubstrate. It doubles and the aforementioned isolation process is performed also to the mesa separation (MESA Isolation) method which embeds a part for this semiconductor layer of a field field, and **********s to an oxide film.

[0004] The silicon-on-insulator desubstrate by the conventional technology which used and manufactured the aforementioned mesa separation method below, and its manufacture method are explained with reference to drawing 1 and drawing 2 . In addition, drawing 1 is the plan and drawing 2 is an II-II'line cross section shown in drawing 1 for explaining the manufacture method.

[0005] With reference to drawing 1 , an active region AR is limited by this semiconductor layer 3 portion of the field field FR embedding, and **********ing to an oxide film 2 so that it may have the shape of an island. The gate electrode 12 is provided with a line form, and the active region which adjoins a longitudinal direction or lengthwise is mutually connected by the aforementioned gate electrode 12.

[0006] With reference to drawing 2 , the SOI substrate 10 which consists of a laminated structure of the base substrate 1, the embedding oxide film 2, and the semiconductor layer 3 is offered. The aforementioned SOI substrate 10 has an active region AR and the isolation field FR, and the aforementioned active region AR is limited by a part for this semiconductor layer of the aforementioned field field FR **********ing to the aforementioned embedding oxide film 2. It is formed in the aforementioned result lifter so that the gate electrode 12 with the gate oxide film 11 may cover the edge of the aforementioned active region AR.

[Translation done.]

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EFFECT OF THE INVENTION

[Effect of the Invention] Above, like explanation, a gate electrode is arranged only on an active region, and since this invention was constituted so that the edge might not be covered, it can prevent generating of the leakage current by the edge effect. Thereby, the increase in an OFF leakage current can be prevented and an element property and reliability can be raised.

[Translation done.]

TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] However, by covering the edge of the aforementioned active region AR by the aforementioned gate electrode 12, the silicon-on-insulator desubstrate by the conventional technology manufactured using the aforementioned mesa separation method makes a leakage current increase, consequently causes the fall of element properties, such as a fall of drive speed.
[0008] In detail, the conventional silicon-on-insulator desubstrate manufactured using the mesa separation method has the gestalt by which the edge of an active region AR was covered by the gate electrode 12, as shown in drawing 2 . In this case, if predetermined voltage is impressed to the aforementioned gate electrode 12, the phenomenon which the electric field by the gate concentrate on the edge of the aforementioned active region AR will be caused. However, in order that concentration of the electric field to the edge of this active region AR may cause the phenomenon in which the channel formed in the edge of the aforementioned active region AR carries out a turn-on (Turn-On) ahead of the channel formed in the aforementioned active-region AR inside consequently, when an OFF leakage current (Off-leakage Current) increases, an element property falls.
[0009] Drawing 3 is a graph which shows the VG-ID curve to the aforementioned silicon-on-insulator desubstrate. In drawing, a solid line shows an actual VG-ID curve including the effect by the edge, and a dotted line shows the VG-ID curve which eliminated the effect by the edge.
[0010] When the channel generated at the edge of an active region carries out a turn-on ahead of the channel generated in the inside portion with reference to drawing 3 , a hump (Hump) occurs with an VG-ID curve. Moreover, if the OFF leakage current at the time of VGS=0V is compared, a leakage current when the effect by the edge shows up is larger than a leakage current when that is not right.
[0011] Thus, when manufacturing a silicon-on-insulator desubstrate using a mesa separation method, preventing the increase in the leakage current by the edge effect is the indispensable technical problem which solves an element property fall.
[0012] Originated in order that this invention may solve the aforementioned technical problem, the purpose is offering a silicon-on-insulator desubstrate without an edge leakage current. Moreover, other purposes of this invention are offering the manufacture method of a silicon-on-insulator desubstrate without an edge leakage current.

[Translation done.]

MEANS

[Means for Solving the Problem] In order to attain the aforementioned purpose, the silicon-on-insulator desubstrate by this invention A base substrate, an embedding oxide film, and the SOI substrate that consists of a laminated structure of a semiconductor layer; so that an active region may be limited So that a part for this semiconductor layer of the aforementioned field field may be touched with the aforementioned embedding oxide film Formed oxide-film; A gate electrode pattern with the gate oxide film formed only on the aforementioned active region; so that between the gate electrode patterns formed in each of the active region arranged by source and drain field; and the single tier which were formed in the active region of the aforementioned semiconductor layer of the both sides of the aforementioned gate electrode pattern may be connected The gate electrode line formed on the aforementioned gate electrode pattern and the field field is included.
[0014] Moreover, the manufacture method of the silicon-on-insulator desubstrate by this invention The stage which forms a gate oxide film and the 1st electric conduction film one by one on the stage; aforementioned semiconductor layer which offers the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an active region may be limited The electric conduction film of the above 1st of this portion of a field field, The stage which carries out the vacuum evaporationo of the oxide film to the stage; aforementioned result lifter which **********s a part for a gate oxide film and a semiconductor layer; until the 1st electric conduction film which carried out [aforementioned] etching is exposed The aforementioned mask pattern is used. The stage which forms the mask pattern of a line gestalt on the electric conduction film of the stage; above 2nd which carries out the vacuum evaporationo of the 2nd electric conduction film on the oxide film by which polish was carried out [aforementioned] with the 1st electric conduction film which ground the aforementioned oxide film and carried out the stage; aforementioned etching; The electric conduction film of the above 2nd, By **********ing, the 1st electric conduction film and gate oxide film which **********ed In the active region of the aforementioned semiconductor layer of the both sides of stage; which forms the gate electrode line which links the gate electrode pattern arranged only on the aforementioned active region, and the gate electrode pattern respectively formed on the adjoining active region arranged by the single tier, and the aforementioned gate electrode line, respectively The source And the stage which forms a drain field is included.
[0015] Furthermore, the manufacture method of the silicon-on-insulator desubstrate by this invention The stage which forms a gate oxide film and the 1st electric conduction film one by one on the stage; aforementioned semiconductor layer which offers the SOI substrate which consists of a laminated structure of a base substrate, an embedding oxide film, and a semiconductor layer; so that an electric conduction line may be formed The stage which forms the source and a drain field respectively in the aforementioned semiconductor layer of the both sides of the stage; aforementioned electric conduction line which carries out patterning of the electric conduction film and the aforementioned gate oxide film of the above 1st; so that an active region may be limited By **********ing, an electric conduction line and a semiconductor layer with the gate oxide film on a field field The stage which carries out the vacuum evaporationo of the oxide film to the stage; aforementioned result lifter which forms a gate electrode pattern only on an active region; until the aforementioned gate electrode pattern is exposed The stage which forms the gate electrode line which links the gate electrode pattern respectively formed on the adjoining active region arranged by the single tier on stage; which grinds the aforementioned oxide film, the aforementioned gate electrode pattern, and the oxide film is included.
[0016] By referring to the following explanation and a drawing, it is better and an understanding of this invention and the form of the operation is attained.
[0017]
[Embodiments of the Invention] Hereafter, based on an accompanying drawing, the suitable example of this invention is explained in detail. Drawing 4 or drawing 9 is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[0018] The SOI substrate 30 which consists of a laminated structure of the semiconductor layer 23 which is arranged on the embedding oxide film 22 which is arranged with reference to drawing 4 on the base substrate 21 which supports the whole, and the aforementioned base substrate 21, and offers perfect isolation, and the aforementioned embedding oxide film 22, and offers an active region is offered. The aforementioned SOI substrate 30 has an active region AR and the field field FR. As for the aforementioned semiconductor layer 23, it is desirable to have the thickness of 100-5,000A. The gate oxide film 31 is formed on the aforementioned semiconductor layer 23, and the vacuum evaporationo of the 1st electric conduction film 32 is carried out on the aforementioned gate oxide film 31. The electric conduction film 32 of the above 1st is a polysilicon contest film desirably.
[0019] It is limited by the mesa separation method which **********s until the aforementioned embedding oxide film 22 exposes a part for the 1st electric conduction film portion by which the active region AR in which an element is formed was formed on the field field FR, a gate oxide-film portion, and a semiconductor layer with reference to drawing 5 . Drawing 10 is a plan corresponding to drawing 5 . As shown in drawing, the 1st electric conduction film 32 which carried out [aforementioned] etching remains only on the aforementioned active region AR.
[0020] With reference to drawing 6 , the vacuum evaporationo of the 1st electric conduction film 32 in which the oxide film 33 carried out [aforementioned] etching is completely carried out to the aforementioned result lifter by sufficient thickness about a wrap. Then, the aforementioned oxide film 33 is ground by the CMP (Chemical Mechanical Polishing) process until the 1st electric conduction film 32 which carried out [aforementioned] etching is exposed. Consequently, the aforementioned oxide film 33 remains only on the field field FR.
[0021] With reference to drawing 7 , vacuum evaporationo is carried out on the oxide film 33 and the 1st electric conduction film 32 which carried out [aforementioned] etching with which polish of the 2nd electric conduction film 34 was carried out [aforementioned]. Here, the electric conduction film 34 of the above 2nd is matter which is the same matter as the electric conduction film 32 of the above 1st, or is different. For example, if the electric conduction film 32 of the above 1st is a polysilicon contest film, as for the electric conduction film 34

of the above 2nd, it is desirable that it is a metal silicide film. The mask pattern 35 which consists of a photoresist is formed with a line gestalt on the electric conduction film 34 of the above 2nd.
[0022] With reference to drawing 8 , when gate electrode line 34a and gate electrode pattern 32a ********** the 2nd electric conduction film, the 1st electric conduction film, and a gate oxide film, using the aforementioned mask pattern (un-illustrating) as an etching mask, it is formed. After an appropriate time, the aforementioned mask pattern is removed.
[0023] Here, since the 1st electric conduction film which remained on the active region AR is formed by **********ing, the aforementioned gate electrode pattern 32a is arranged only on the aforementioned active region AR. On the other hand, the aforementioned gate electrode line 34a is arranged also on the field field FR as well as an aforementioned gate electrode pattern 32a top so that between the gate electrode patterns respectively formed on the adjoining active region AR arranged by the single tier may be connected mutually [drawing 11 (a) and 11 (b)].
[0024] With reference to drawing 9 , the source and the drain fields 36 and 37 are formed in the semiconductor layer part of the both sides of the aforementioned gate electrode line 34a of the ion-implantation process using the aforementioned gate electrode line 34a as a mask. Consequently, a silicon-on-insulator desubstrate like a transistor is completed.
[0025] In the silicon-on-insulator desubstrate by this invention manufactured according to the aforementioned process, since the gate electrode which consists of a gate electrode pattern and a gate electrode line is only formed only on an active region and is formed in the structure which does not cover the edge of an active region, the leakage current by the turn-on of the channel being previously carried out at the edge of the aforementioned active region is not generated. Therefore, since the silicon-on-insulator desubstrate by this invention can prevent the increase in the OFF leakage current by the edge effect, it can raise the property and reliability.
[0026] Drawing 12 or drawing 16 is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention. Here, the same sign shows the same portion as a previous example.
[0027] With reference to drawing 12 , the SOI substrate 30 which consists of a laminated structure of the base substrate 21, the embedding oxide film 22, and the semiconductor layer 23 is offered, and the gate oxide film 31 and the 1st electric conduction film 42 are formed one by one on the aforementioned semiconductor layer 23. Patterning of the electric conduction film 42 and the gate oxide film 31 of the above 1st is carried out so that it may have a line form (refer to drawing 17).
[0028] The source and the drain fields 36 and 37 are formed in the semiconductor layer part of the both sides of the electric conduction film 42 of the above 1st of the ion-implantation process using the 1st electric conduction film 42 by which patterning was carried out [aforementioned] as a mask.
[0029] It is formed so that the mask pattern 50 which consists of a photoresist may cover an active region AR to the aforementioned result lifter with reference to drawing 13 .
[0030] With reference to drawing 14 , an active region AR is limited by **********ing until it embeds a part for the semiconductor layer exposed using the aforementioned mask pattern (un-illustrating) and an oxide film 22 is exposed. At this time, between the aforementioned etching, it is formed so that gate electrode pattern 42a in which it **********s, consequently the 1st electric conduction film and gate oxide-film portion which were formed on the field field FR have [both] a gate oxide film may be arranged only on the aforementioned active region AR. After an appropriate time, the aforementioned mask pattern is removed.
[0031] Drawing 18 is a plan corresponding to aforementioned drawing 14 which shows the result of the aforementioned process. As shown in drawing, the aforementioned gate electrode pattern 42a is arranged only on an active region AR.
[0032] With reference to drawing 15 , the vacuum evaporationo of the oxide film 33 is carried out to the aforementioned result lifter, and it is ground by the CMP process until the upper surface of the aforementioned gate electrode pattern 42a is exposed after that.
[0033] With reference to drawing 16 , the vacuum evaporationo of the 2nd electric conduction film is carried out to the aforementioned result lifter, and gate electrode line 44a is formed by carrying out patterning of the electric conduction film of the above 2nd after that. The aforementioned gate electrode line 44a is formed so that the gate electrode pattern respectively formed on the adjoining active region AR arranged by the single tier like the previous example may be linked.
[0034] The aforementioned gate electrode line 44a can be formed with the different quality of the material from the aforementioned gate electrode pattern 42a. For example, when the aforementioned gate electrode pattern 42a is formed by the polysilicon contest film, as for the aforementioned gate electrode line 44a, forming by the metal silicide film is desirable.
[0035] Moreover, the aforementioned gate electrode line 44a can be formed with the same quality of the material as the aforementioned gate electrode pattern 42a. In this case, since the gate oxide film 31 as shown in drawing 19 by incorrect alignment is exposed at the time of etching for forming the aforementioned gate electrode line 44a, the reliability of an element falls. Therefore, when formed with the same quality of the material as the aforementioned gate electrode pattern 42a, it is desirable [the aforementioned gate line 44a] to be formed more sharply than the aforementioned gate electrode pattern 42a so that exposure of the gate oxide film 31 by incorrect alignment may be prevented.
[0036] In addition, it is possible to Oshi to carry out change implementation within limits which this invention is not limited to the aforementioned example and do not deviate from the meaning of this invention.

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the plan showing the silicon-on-insulator desubstrate by the conventional technology manufactured using the mesa separation method.
[Drawing 2] It is the cross section which meets the II-II'line shown in drawing 1 for explaining the manufacture method of the aforementioned silicon-on-insulator desubstrate.
[Drawing 3] It is the VG-ID curve which shows the change of drain current to a gate voltage.
[Drawing 4] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[Drawing 5] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[Drawing 6] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[Drawing 7] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[Drawing 8] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[Drawing 9] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by the example of this invention.
[Drawing 10] It is a plan corresponding to drawing 5 .
[Drawing 11] (a) is a plan corresponding to drawing 8 , and (b) is a cross section which meets the Y-Y'line of (a).
[Drawing 12] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention.
[Drawing 13] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention.
[Drawing 14] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention.
[Drawing 15] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention.
[Drawing 16] It is a cross section for explaining the manufacture method of the silicon-on-insulator desubstrate by other examples of this invention.
[Drawing 17] It is a plan corresponding to drawing 12 .
[Drawing 18] It is a plan corresponding to drawing 14 .
[Drawing 19] It is the cross section showing the state where the incorrect alignment between the gate electrode lines and gate ** patterns which were formed of other examples of this invention occurred.
[Description of Notations]
21 Base Substrate
22 Embedding Oxide Film
23 Semiconductor Layer
30 SOI Substrate
31 Gate Oxide Film
32 42 1st electric conduction film
32a, 42a Gate electrode pattern
33 Oxide Film
34 2nd Electric Conduction Film
34a, 44a Gate electrode line
35 50 Mask pattern
36 Source Field
37 Drain Field

[Translation done.]

* NOTICES *

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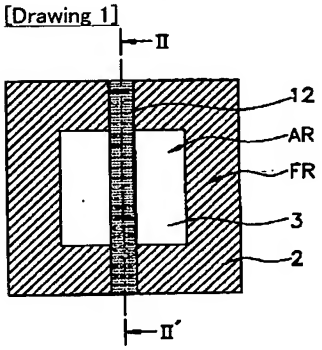
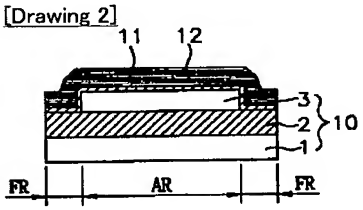
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

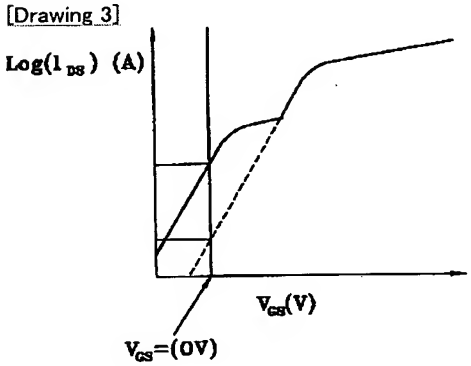
[Drawing 1]



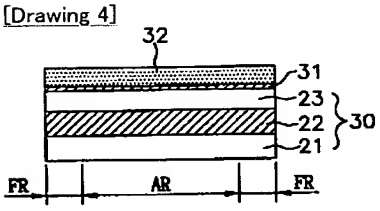
[Drawing 2]



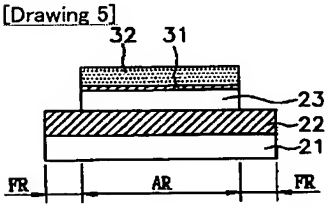
[Drawing 3]



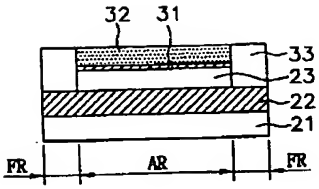
[Drawing 4]



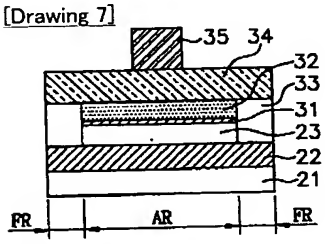
[Drawing 5]



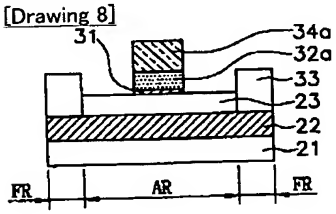
[Drawing 6]



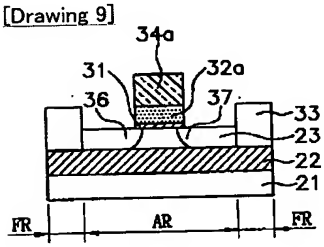
[Drawing 7]



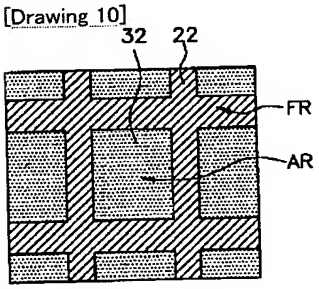
[Drawing 8]



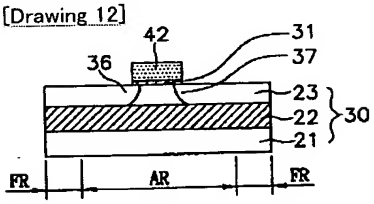
[Drawing 9]



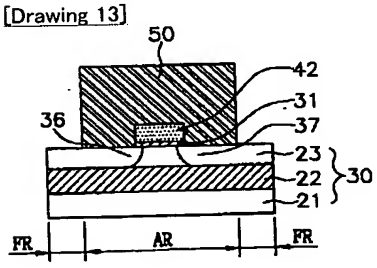
[Drawing 10]



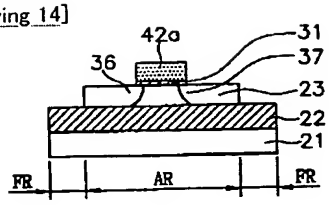
[Drawing 12]



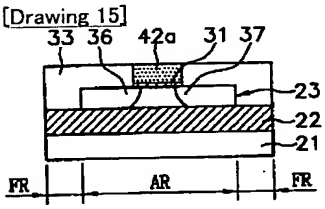
[Drawing 13]



[Drawing 14]

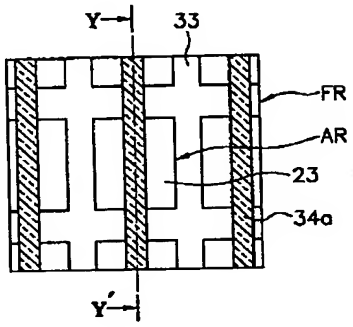


[Drawing 15]

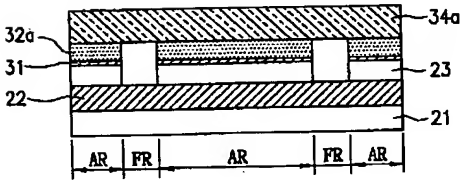


[Drawing 11]

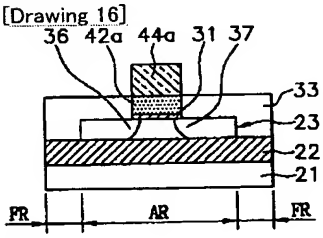
(a)



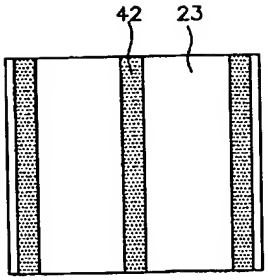
(b)



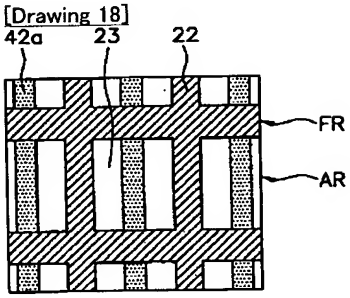
[Drawing 16]



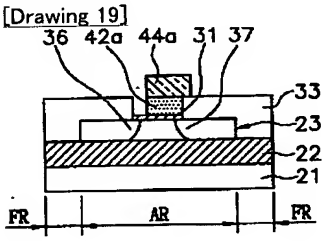
[Drawing 17]



[Drawing 18]



[Drawing 19]



[Translation done.]